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Analyzing the Energy-Time in High-Performance Heterogeneous Computing Applications: using scheduling algorithm

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Abstract: In nowadays, users of high-performance heterogeneous computing are most interested in raw performance, both energy and power consumption have become elucidative concerns. One approach to lowering energy and power is to use high-performance cluster nodes that have sundry power-performance states so that the energy-time trade-off can be dynamically adjusted.HPC is always been performance-oriented. However, a consequence of the push towards maximum performance is increased energy consumption, mostly in datacenters and supercomputing centers. Recently, more and more people are focused on the energy efficiency of HPC centers. The power consumption of supercomputer listed in the first 10 of top 500 CPU cycle is generally more than 1Mkw. Power-aware methods have been widely used in data center or supercomputer center for reducing the power consumption. It is convenient for us to reduce the power consumption with frequency scalable CPU being adopted in the HPC centers. In this paper, we study the effects of memory and communication bottlenecks via direct measurement of time and energy. Firstly, we identify the application as different kinds of power consumption by the load balancing and communication time. High performance, power-aware computing (HPPAC) will present research based on power consumption, energy consumption, with little or no performance penalty in high-performance computing systems. We also used efficient application scheduling algorithm for achieving high performance and low power consumption system in heterogeneous computing (HC) environments.

Keywords: power-energy aware, DAG, high-performance heterogeneous computing.

1. INTRODUCTION

High-performance computing (HPC) likely to push performance at all costs. The Earth Simulator, one of the world's fastest supercomputers, utilize 7 MW of power. It is unlikely that supercomputing centers can continue increasing consumption of assets. In particular, energy consumption and their sultan heat dissipation is becoming an important limiting factor for energy aware system. Reducing energy saves money and increases reliability. As a result, low-power high-performance clusters have been come into existence.

Power-performance optimization involves minimizing the present efficiency gap in processing throughput and power utilization. Energy efficiency, a new focus for general-purpose computing, has been a major technology driver in the application of mobile and embedded areas for some time. Earlier work emphasized extending battery life of system, but it has since expanded to include peak power reduction because thermal constraints began to limit further CPU performance enhancements. Energy management has now become a key issue for servers and data center operations, focusing on the lowering of all energy-related costs, including capital, operating expenses, and environmental impacts. It is possible to bring down power consumption without a significant increase in execution time because an increase in CPU frequency usually results in a smaller increase in application performance. The reason for this is that the CPU is not consistently the bottleneck resource. Therefore, growing frequency also increases CPU stalls. According to

Eric Schmidt, CEO of Google, the great problem to Google "is not speed but power—low power, because data centers can swallow as much electricity as a city" In past years, more and more attention focuses on the scheduling problem of applications on heterogeneous computing system. A heterogeneous computing (HC) system is described as a

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distributed suite of computing machines with distinct capabilities interconnected by different high speed links utilized to executed parallel applications. Duplication-based algorithm is a kind of efficient algorithm to minimize the power and maximize the performance by assigning a task to several processors, which reduces the intercommunication between tasks.

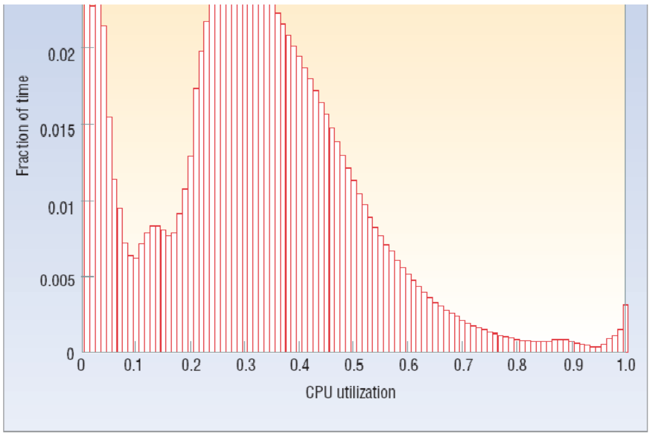

Figure 1. Average CPU utilization

This paper is partly based on previously published works. it explores energy-time trade-off in mobile systems. we develop techniques for increasing throughput by improving the power/energy efficiency of nodes in data centers. we propose a new energy aware scheduling algorithm aiming at reducing the energy consumption of duplication-based algorithms. Through the analysis on the duplication-based algorithms, we find that some copies of tasks can be deleted, which do not affect the task precedence but can reduce energy consumption greatly.It investigates the trade-off between energy and capacity (execution time) for HPC applications on a real small-scale power-scalable cluster. we assume that all information of applications including execution time of tasks, the data size of communication between tasks, and task dependencies are known a priori, which is represented with a static scheduling. Static task scheduling takes place during compile time before tasks execution.

2. Related Work

In recent years, the research of power management has been a hot spot. It covers the servers, cluster systems, mobile systems, storage systems, dynamic load balancing, dynamic adjustment of CPU frequency, scheduling algorithm etc. The work mentioned in this paper is similar to CPU frequency-dependent dynamic regulation, application based power-aware system.

The various systems are below:

A. Server/Cluster Systems

In paper, it proposed a resource allocation algorithm, which using of greedy algorithm approach to adjust the number of resources, reallocation, utilization, balance demand and supply of resources in order to achieve optimal utilization of resources.

In recent its main contributions are:

1) A provision of services through dynamic request to redirect resources. In this mode, it is able to reduce overall system power consumption and guarantees service level agreements at the same time.

2) For each service in the mean load level, it proposed a simple strategy for dynamic adjustment of resources to reduce the excessive use of resources.
3) Through its economic framework model, it can achieve a certain balance for the service quality and lower power consumption.

B. Mobile system

Energy efficiency in mobile computing platforms has become a very important and challenging problem. It proposed a novel dynamic software management (DSOM) framework to improve battery utilization. The design and implementation of a DSOM module in the user space is independent of the operating system (OS). It is satisfied with the quality of service(QoS) while reducing overall system power consumption. In many applications, it uses priority based pre-emptive strategy, in order to avoid competing for limited energy resources.

C. Dynamic Frequency and Voltage Scaling

Nowadays, the computer hardware manufacturers are more concerned about the energy consumption of various computer components, current main computer components such as CPU, memory, hard disks, etc, have the energy adjustable functions. CPU is at the largest share of energy consumption in the common computer system, so we use various methodology to adjust CPU frequency and voltage to reduce the energy consumption of the above.
Additionally, an examination of energy efficiency and operating points shows that the most energy-efficient gear does not always result in the underperformance point. Some practices estimate power consumption using performance counters. In a high-performance processor, a dominant segment of power consumption is due to use of instruction level parallelism (ILP).

3. Model

A scheduling system model consists of a HPC environment, an application and performance criteria for scheduling. In this section, we will present computing system model, application model and performance criteria models related to power aware.

A. Computing System Model

The computing system considered in this paper is heterogeneous. Let for example, we take $P = \{P_k | 0 \leq k \leq n - 1\}$ be a set of n processors with different capacities. The capacity of each processor processing tasks depends on how well the architecture of the processor matches tasks' processing requirements. A task scheduled on its best-suited processor will send shorter execution time than on a less-suited processor. The best processor for one piece of work may be the worst processor for another task.

B. Application Model

A Directed Acyclic Graph (DAG) G(V, E, $[w_{i,k}]$) consists of a set of nodes $V = \{v_i | 0 \leq i \leq m - 1\}$ representing the tasks in an application and a set of directed edges E indicating dependencies between tasks. Let $c_{i,j}$ be the weight of edge $e_{i,j}$, which shows the required communication time to send data from v_i to v_j. Here v_i is called the parent of v_j . $[w_{i,k}]$ is a $m \times n$ matrix of computation time, where $w_{i,k}$ presents the computation. time of task v_i executed on processor pk for 0 ≤ i ≤ m−1 and 0 ≤ k ≤ n − 1. Fig. 1 gives a DAG to represent the application model, and Table lists the computation time matrix [wi,k].

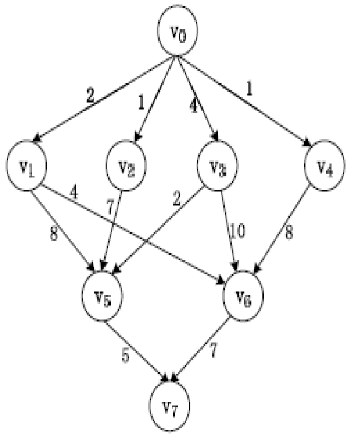

Figure 2. DAG Representation

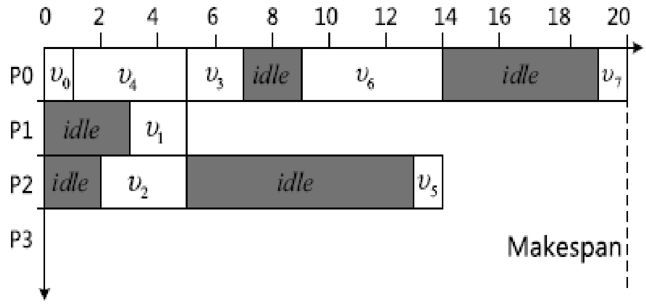

Figure 3. Schedule of DAG

Task node	p_0	p_1	p_2	p_3	$\overline{w_i}$	$rank_u$
v_0	1	1	2	1	1.25	32.00
v_1	3	2	4	2	2.75	19.75
v_2	5	6	3	4	4.5	20.50
v_3	2	4	4	2	3.0	26.75
v_4	4	8	7	8	6.75	28.5
v_5	3	3	1	2	2.25	9.00
v_6	5	5	5	5	5	13.75
v_7	1	2	2	2	1.75	1.75

Figure 4. Computation cost matrix

C. Performance Criteria

Makespan is a main criterion to measure the performance of scheduling algorithms. For a task vi scheduled on processor pk, st(vi, pk) and ft(vi, pk) present the start time and finish time of task vi on pk.Because preemptive execution is not allowed, ft(vi, pk) = st(vi, pk) + wi,k. Makespan is denoted as makespan = ft(vexit). The proposed algorithm in this paper is to reduce the energy consumption of a valid schedule generated by duplication-based algorithms without degrading the makespan, so we introduce the energy consumption model used in this paper.

4. Future Work

We can use various scheduling based method for improving performance criteria and energy-consumption. we measure the time complexity of algorithm for analysis. We plan to further investigate the extension of ECS to grid environments in which the availability and capacity of resources fluctuates. Therefore, the accurate completion time of a task on a particular processor is difficult, if not impossible, to determine a priori.

5. Conclusion

In summary, this paper proffers the methodology, design, and evaluation of performance-directed, system-wide, for high performance computing. Typically, the makespan of a task graph generated by a scheduling algorithm is used as the main performance measure; however, as our algorithm is proposed on the basis of duplication based algorithms, and has the same performance on makespan with those algorithms. The amount of energy savings is affected by many factors, such as the number of processors, CCR and parallelism level. For the fixed number of tasks, the amount of energy savings increases with the increasing number of processors caused by the increase of idle time and duplications.

REFERENES

1. vincent w. Freeh, david k. Lowenthal, feng pan, nandini kappiah, Rob springer, barry l. Rountree, and mark e. Femal, member, ieee transactions on parallel and distributed systems, vol. 18, no. 6, june 2007.
2. Jing Mei, ∗Kenli Li National Supercomputing Center in Changsha College of Information Science and Enginnering, Hunan University, 2012 ACM/IEEE 13th International Conference on Grid Computing.
3. Young Choon Lee and Albert Y. Zomaya Advanced Networks Research Group, School of Information Technologies the University of Sydney NSW 2006, Australia, 9th IEEE/ACM International Symposium on Cluster Computing and the Grid.
4. Feng, R. Ge, K. W. Cameron. Power and Energy Profiling of Scientific Applications on Distributed Systems. In Proceedings of IPDPS'05, Denver, CA, April 2005.